What is Claimed is:

1. An integrated circuit electrode comprising:

an alloy comprising a first metal and a second metal having lower work function than the first metal.

2. An integrated circuit electrode according to Claim 1 wherein the second metal also has higher oxygen affinity than the first metal.

3. An integrated circuit electrode according to Claim 1 wherein the first metal is selected from the group consisting of Co, Ni, Pd, Rh, Ru, Ir, Pt, Au, Re, Os, RuO_2, IrO_2 and alloys thereof and wherein the second metal is selected from the group consisting of Mn, Mg, V, Ti, Cr, Y, Zr, Ta, La, Gd, Sm, Pr, Nb, Al, Hf and alloys thereof.

4. An integrated circuit electrode according to Claim 1 wherein the first metal is Ru and the second metal is Ta.

5. An integrated circuit electrode according to Claim 1 in combination with spaced apart source and drain regions in an integrated circuit substrate and a gate insulating region on the integrated circuit substrate between the spaced apart source and drain regions, wherein the integrated circuit electrode is on the gate insulating region opposite the integrated circuit substrate to provide an integrated circuit field effect transistor.

6. An integrated circuit electrode according to Claim 5 wherein the spaced apart source and drain regions are first spaced apart source and drain regions, wherein the gate insulating region is a first gate insulating region and wherein the integrated circuit electrode is a first gate electrode, in further combination with:

second spaced apart source and drain regions in the integrated circuit substrate and of opposite conductivity type than the first spaced apart source and drain regions;

a second gate insulating region on the integrated circuit substrate between the second spaced apart source and drain regions; and

a second gate electrode on the second gate insulating region opposite the integrated circuit substrate, wherein the second gate electrode comprises the first metal.

7. An integrated circuit electrode according to Claim 6 wherein the second gate electrode is free of the second metal.

8. An integrated circuit electrode according to Claim 6 wherein the second gate electrode comprises an alloy comprising the first metal and the second metal.

9. An integrated circuit electrode according to Claim 6 wherein the second gate electrode comprises an alloy comprising the first metal and the second metal and having different amounts of the first metal relative to the second metal than the first gate electrode.

10. An integrated circuit electrode according to Claim 7 wherein the first spaced apart source and drain regions are n-type spaced apart source and drain regions and wherein the second spaced apart source and drain regions are p-type spaced apart source and drain regions.

11. An integrated circuit electrode according to Claim 9 wherein the first spaced apart source and drain regions are n-type spaced apart source and drain regions, wherein the second spaced apart source and drain regions are p-type spaced apart source and drain regions and wherein the second gate electrode comprises a higher percentage of the first metal relative to the second metal than the first gate electrode.

12. An integrated circuit electrode according to Claim 11 wherein the first gate electrode comprises an Ru-Ta alloy having between about 40% Ta and about 54% Ta and wherein the second gate electrode comprises an Ru-Ta alloy having less than about 20% Ta.

13. An integrated circuit electrode according to Claim 11 wherein the first gate electrode comprises an Ru-Ta alloy having at least about 30% Ta and wherein the second gate electrode comprises an Ru-Ta alloy having less than about 30% Ta.

14. An integrated circuit electrode according to Claim 5 wherein the gate insulating region is a first gate insulating region and wherein the integrated circuit electrode is a first gate electrode, in further combination with:

a second gate insulating region on the integrated circuit substrate between the spaced apart source and drain regions; and

a second gate electrode on the second gate insulating region opposite the integrated circuit substrate, wherein the second gate electrode comprises an alloy comprising a first metal and a second metal having lower work function than the first metal to provide a multiple gate integrated circuit field effect transistor.

15. An integrated circuit electrode according to Claim 1 wherein the first metal has a work function of greater than about 4.5eV and wherein the second metal has a work function of less than about 4.5eV.

16. An integrated circuit electrode according to Claim 1 wherein the first metal has a work function of about 5eV and wherein the second metal has a work function of about 4eV.

17. An integrated circuit electrode according to Claim 1 wherein the first metal has a work function of between about 5eV and about 5.2eV and wherein the second metal has a work function of between about 4eV and about 4.1eV.

18. An integrated circuit electrode according to Claim 1 wherein the first metal has a work function of between about 5eV and about 5.2eV and wherein the second metal has a work function of between about 3.5eV and about 4.0eV.

19. A method of fabricating an integrated circuit electrode comprising:

coforming an alloy comprising a first metal and a second metal having lower work function than the first metal on an integrated circuit substrate to thereby form an integrated circuit electrode on the integrated circuit substrate.

20. A method according to Claim 19 wherein the coforming comprises coforming an alloy comprising a first metal and a second metal having lower work function and higher oxygen affinity than the first metal on the integrated circuit substrate.

21. A method according to Claim 19 wherein the first metal is selected from the group consisting of Co, Ni, Pd, Rh, Ru, Ir, Pt, Au, Re, Os, RuO_2, IrO_2 and alloys thereof and wherein the second metal is selected from the group consisting of Mn, Mg, V, Ti, Cr, Y, Zr, Ta, La, Gd, Sm, Pr, Nb, Al, Hf and alloys thereof.

22. A method according to Claim 19 wherein the first metal is Ru and the second metal is Ta.

23. A method according to Claim 19 further comprising:

fabricating spaced apart source and drain regions in the integrated circuit substrate and a gate insulating region on the integrated circuit substrate between the spaced apart source and drain regions, wherein the integrated circuit electrode is on the gate insulating region opposite the integrated circuit substrate to provide an integrated circuit field effect transistor.

24. A method according to Claim 19 wherein the spaced apart source and drain regions are first spaced apart source and drain regions, wherein the gate insulating region is a first gate insulating region and wherein the integrated circuit electrode is a first gate electrode, the method further comprising:

fabricating second spaced apart source and drain regions in the integrated circuit substrate and of opposite conductivity type than the first spaced apart source and drain regions, a second gate insulating region on the integrated circuit substrate between the second spaced apart source and drain regions and a second gate electrode on the second gate insulating region opposite the integrated circuit substrate, wherein the second gate electrode comprises the first metal.

25. A method according to Claim 24 wherein the second gate electrode is free of the second metal.

26. A method according to Claim 24 wherein the second gate electrode comprises an alloy comprising the first metal and the second metal.

27. A method according to Claim 24 wherein the second gate electrode comprises an alloy comprising the first metal and the second metal having different amounts of the first metal relative to the second metal than the first gate electrode.

28. A method according to Claim 25 wherein the first spaced apart source and drain regions are n-type spaced apart source and drain regions and wherein the second spaced apart source and drain regions are p-type spaced apart source and drain regions.

29. A method according to Claim 27 wherein the first spaced apart source and drain regions are n-type spaced apart source and drain regions, wherein the second spaced apart source and drain regions are p-type spaced apart source and drain regions and wherein the second gate electrode comprises a higher percentage of the first metal relative to the second metal than the first gate electrode.

30. A method according to Claim 29 wherein the first gate electrode comprises an Ru-Ta alloy having between about 40% Ta and about 54% Ta and wherein the second gate electrode comprises an Ru-Ta alloy having less than about 20% Ta.

31. A method according to Claim 29 wherein the first gate electrode comprises an Ru-Ta alloy having at least about 30% Ta and wherein the second gate electrode comprises an Ru-Ta alloy having less than about 30% Ta.

32. A method according to Claim 19 wherein the gate insulating region is a first gate insulating region and wherein the integrated circuit electrode is a first gate electrode, the method further comprising:

fabricating a second gate insulating region on the integrated circuit substrate between the spaced apart source and drain regions and a second gate electrode on the second gate insulating region opposite the integrated circuit substrate, wherein the

second gate electrode comprises an alloy comprising a first metal and a second metal having lower work function than the first metal to provide a multiple gate integrated circuit field effect transistor.

33. A method according to Claim 19 wherein the first metal has a work function of greater than about 4.5eV and wherein the second metal has a work function of less than about 4.5eV.

34. A method according to Claim 19 wherein the first metal has a work function of about 5eV and wherein the second metal has a work function of about 4eV.

35. A method according to Claim 19 wherein the first metal has a work function of between about 5eV and about 5.2eV and wherein the second metal has a work function of between about 4eV and about 4.1eV.

36. A method according to Claim 26 wherein the first metal has a work function of between about 5eV and about 5.2eV and wherein the second metal has a work function of between about 3.5eV and about 4.0eV.

37. A method according to Claim 19 wherein the coforming comprises cosputtering the alloy comprising the first metal and the second metal having lower work function than the first metal on the integrated circuit substrate.

38. A method according to Claim 27:

wherein the coforming comprises cosputtering the alloy comprising the first metal and the second metal having lower work function than the first metal on the integrated circuit substrate from a first sputtering target that includes the first metal and a second sputtering target that includes the second metal; and

wherein the fabricating a second gate electrode on the second gate insulating region opposite the substrate comprises cosputtering the alloy comprising the first metal and the second metal having lower work function than the first metal on the integrated circuit substrate from the first sputtering target and the second sputtering target and at a different sputtering power than for the coforming.